

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. 501.43228X00	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT MURATA, et al.	
		FILING DATE January 14, 2004	GROUP

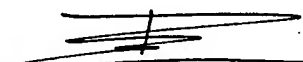
U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
TL	AA 5,198,683	03/30/1993	SIVAN	357	67	05/03/1991
TL	AB 5,670,803	09/23/1997	BEILSTEIN, Jr. et al.	257	278	02/08/1995
TL	AC 5,994,735	11/30/1999	MAEDA, et al.	257	329	11/30/1999
TL	AD 5,627,390	05/06/1997	MAEDA, et al.	257	302	05/06/1997
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	AI					
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	AK					
	AL					

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Abstract	
						Yes	No
TL	AM 11-176936	07/02/1999	JP	H01L	21/768	X	
	AN 9-232447	09/05/1997	JP	H01L	21/8244	X	
	AO 2001-28443	01/30/2001	JP	H01L	29/786	X	
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TL	AR 00/70683	11/23/2000	WO	H01L	27/108		
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	AT						

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TL	AU	WATANABE, et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995
	AV	
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Examiner 		Date Considered 07/05/05